Lab 3 – Characterization of S Parameters of a Packaged Transistor

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# EEL5439C RF and Microwave Active Circuits

Prof. Dr. Kenle Chen - Section 0012

# 3/7/2024 – 3/14/2024



# **Experiment Objective**

The objective of this lab is to understand the S-Parameter extraction from realistic transistor and compare with foundry-supplied model.

# 2.0 Experiment Procedure

A computer diagram with many symbols

Description automatically generated with medium confidence

Power Amplifier Schematic

A computer generated image of a rectangular object

Description automatically generated

Power Amplifier Layout

A diagram of a diagram

Description automatically generated

Power Amplifier Symbol in ADS

A computer screen shot of a circuit board

Description automatically generated

Power Amplifier Symbol Port in ADS

1. Show how to design the bias network and the component values.

A diagram of a circuit

Description automatically generated

DC Bias Design Equation

For highest gain, should be 20 mA, given this condition and that (from datasheet). The design equations can be utilized to compute the biasing resistor values.

1. Plot all S parameters (in dB) over the full frequency range.

A screenshot of a graph

Description automatically generated

Layout S-Param Smith Chart

A graph of a function

Description automatically generated

Layout S-Param Tabular

A screenshot of a screen

Description automatically generated

Schematic S-Param Smith Chart

A graph of a function

Description automatically generated with medium confidence

Schematic S-Param Tabular Chart

A screenshot of a screen

Description automatically generated

Measured S-Param Smith Chart

A graph of a function

Description automatically generated with medium confidence

Measured S-Param Tabular Chart

1. Identify the gain of this mismatched transistor at 1 GHz. Also calculate VSWRin and VSWRout.

A black and white text

Description automatically generated

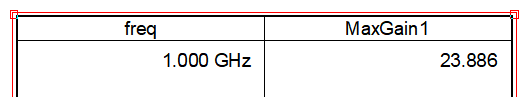
Max Gain – Layout

A black text with numbers

Description automatically generated with medium confidence

Layout – Scattering Parameters

Layout: and



Max Gain – Schematic

A black text with numbers

Description automatically generated with medium confidence

Schematic Scattering Parameter used to Computer VSWR

Schematic: and

A graph of a graph of a graph of a graph of a graph of a graph of a graph of a graph of a graph of a graph of a graph of a graph of a graph of

Description automatically generated

Measured Scattering Parameters used to Computer Scattering Parameters

*Measured:*  and

1. Plot the input and output impedance versus frequency of the transistor. What are their values at 1 GHz?

A graph of a function

Description automatically generated with medium confidence

Schematic Port Impedance

A screenshot of a graph

Description automatically generated

Layout Port Impedance

A graph of a function

Description automatically generated with medium confidence

Measurements Port Impedance

1. Compare the measurement data with the raw model and post-layout model. For this, you may need to compare the phase in addition to the magnitude. Comment on the possible causes of the difference.

The real part of the schematic port impedance is the highest compared to the layout and the measurements, however, the schematic matches more closely to the measurements compared to the layout. The phase of the schematic and measurement is relatively close; however, the layout has lower phase value compared to the either plot. A possible reason for the deviations in layout plots is that the simulation may not have been as accurate because FEM simulation mode was not utilized. A full EM wave solution would provide a more accurate result. In addition, there are several approximations done with the schematic simulation which will lead to deviation from physical expectations. For the physical measurements, the transistor parameters will drift with each transistor due to variations in the process.

1. Plot |Δ| and K over full frequency range and determine the stability of the transistor at 1 GHz.

A screenshot of a graph

Description automatically generated

Layout Stability Factor and |Delta| Factor.

A graph and diagram of a graph

Description automatically generated with medium confidence

Measured Stability Factor and |Delta| Factor.

A graph of a function

Description automatically generated

Schematic Stability Factor and |Delta| Factor.

1. If the transistor is potentially unstable at 1 GHz, draw the input and output stability circles in the smith chart.

A circular graph with numbers and lines

Description automatically generated with medium confidence

Stability Circles of Layout

A graph of a circular object

Description automatically generated with medium confidence

Stability Circles of Schematic

1. What is the possible consequence if you set the power level too high? What are other possible options to protect the VNA when you measure an active device? Finally, what is the price for a VNA like the one you are using? (If you are in charge of a lab, you will definitely need to know this information.)

Setting the power level too high can damage the transistor/PCB, RF transistors can be expensive (several thousands per transistor). However, a more important impact is damage to the VNA equipment. VNA has a maximum power handling level. Damaging a VNA is a very expensive mistake because the cheapest VNAs are several thousands of dollars and often they can be in hundreds of thousands of dollars (sometimes millions of dollars). I have personally worked with a VNA that is $90k USD. A method to protect the VNA is to reduce the power output by using an attenuator.

# 4.0 Conclusion

In conclusion, the characterization of S parameters of a packaged transistor serves as an important step in understanding performance characteristics and ensuring optimal design in RF and microwave active circuits.

One key takeaway from our analysis is the importance of the biasing circuit in Power Amplifier (PA) design. It is imperative that the biasing circuit is less sensitive to parameters such as to avoid stability issues arising from temperature and process variations. Stability concerns extend beyond biasing, as the transistor must also exhibit relative stability outside of the center frequency to prevent oscillation.

Discrepancies observed between simulation and measurement data underscore the complexity of accurately modeling real-world behavior. Factors such as the utilization of FEM simulation mode and inherent approximations in schematic simulations contribute to deviations from physical expectations. Furthermore, variations in transistor parameters due to process discrepancies highlight the need for robust design strategies that account for such variability.

Evaluation of stability factors and delta factors help explain into the transistor's behavior, determine potential instability issues. In cases where instability is detected, measures such as plotting stability circles can guide mitigation efforts to ensure reliable circuit operation.

In summary, this lab experiment has provided valuable insights into the characterization of S parameters of a PA transistor, highlighting the importance of robust design strategies, and careful consideration of biasing circuitry.